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Les documents ci-joints sont conformes aux pièces originales relative à la demande de brevet spécifiée aux pages suivantes, déposées auprès de l'Office soussigné, en tant qu'Office récepteur au sens de l'article 10 du Traité de coopération en matière de brevets (PCT).

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It is hereby confirmed that the attached documents are corresponding with the original pages of the international application, as identified on the following pages, filed under Article 10 of the Patent Cooperation Treaty (PCT) at the receiving office named below.

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Bern, 9 septembre 2002

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**PCT REQUEST**  13-16.B.WO-1

Original (for SUBMISSION) - printed on 19.03.2002 06:29:13 PM

| | | |
|---|---|---|
| 0 | For receiving Office use only | |
| 0-1 | International Application No. | PCT/CH 02 / 00165 |
| 0-2 | International Filing Date | 20. März 2002 (20.03.02) |
| 0-3 | Name of receiving Office and "PCT International Application" | RO / CH - Demande international PCT |
| 0-4 | Form - PCT/RO/101 PCT Request | |
| 0-4-1 | Prepared using | PCT-EASY Version 2.92 (updated 01.01.2002) |
| 0-5 | Petition<br>The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty | |
| 0-6 | Receiving Office (specified by the applicant) | Swiss Federal Intellectual Property Institute (RO/CH) |
| 0-7 | Applicant's or agent's file reference | 13-16.B.WO-1 |
| I | Title of invention | DEVICE ARCHITECTURES WITH SUSPENDED METAL MEMBRANES |
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| | | |
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| V | **Designation of States** | |
| V-1 | Regional Patent<br>(other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned) | AP: GH GM KE LS MW MZ SD SL SZ TZ UG ZM ZW and any other State which is a Contracting State of the Harare Protocol and of the PCT<br>EA: AM AZ BY KG KZ MD RU TJ TM and any other State which is a Contracting State of the Eurasian Patent Convention and of the PCT<br>EP: AT BE CH&LI CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR and any other State which is a Contracting State of the European Patent Convention and of the PCT<br>OA: BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG and any other State which is a member State of OAPI and a Contracting State of the PCT |
| V-2 | National Patent<br>(other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned) | AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH&LI CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG US UZ VN YU ZA ZM ZW |

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|---|---|---|---|
| V-5 | **Precautionary Designation Statement**<br>In addition to the designations made under items V-1, V-2 and V-3, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except any designation(s) of the State(s) indicated under item V-6 below. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit. | | |
| V-6 | **Exclusion(s) from precautionary designations** | NONE | |
| VI | **Priority claim** | NONE | |
| VII-1 | **International Searching Authority Chosen** | European Patent Office (EPO) (ISA/EP) | |
| VIII | **Declarations** | Number of declarations | |
| VIII-1 | Declaration as to the identity of the inventor | - | |
| VIII-2 | Declaration as to the applicant's entitlement, as at the international filing date, to apply for and be granted a patent | - | |
| VIII-3 | Declaration as to the applicant's entitlement, as at the international filing date, to claim the priority of the earlier application | - | |
| VIII-4 | Declaration of inventorship (only for the purposes of the designation of the United States of America) | - | |
| VIII-5 | Declaration as to non-prejudicial disclosures or exceptions to lack of novelty | - | |
| IX | **Check list** | number of sheets | electronic file(s) attached |
| IX-1 | Request (including declaration sheets) | 5 | - |
| IX-2 | Description | 16 | - |
| IX-3 | Claims | 4 | - |
| IX-4 | Abstract | 1 | EZABST00.TXT |
| IX-5 | Drawings | 9 | - |
| IX-7 | TOTAL | 35 | |
| | **Accompanying Items** | paper document(s) attached | electronic file(s) attached |
| IX-8 | Fee calculation sheet | ✓ | - |
| IX-17 | PCT-EASY diskette | - | Diskette |
| IX-19 | **Figure of the drawings which should accompany the abstract** | 1 | |
| IX-20 | **Language of filing of the international application** | English | |
| X-1 | **Signature of applicant, agent or common representative** | | |
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|---|---|---|
| 10-1 | **Date of actual receipt of the purported international application** | 20. März 2002 (20.03.02) |

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|---|---|---|
| 10-2 | Drawings: | |
| 10-2-1 | Received | |
| 10-2-2 | ~~Not received~~ | |
| 10-3 | Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application | |
| 10-4 | Date of timely receipt of the required corrections under PCT Article 11(2) | |
| 10-5 | International Searching Authority | ISA/EP |
| 10-6 | Transmittal of search copy delayed until search fee is paid | X |

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# Device Architectures with Suspended Metal Membranes

## Field of the invention

This invention concerns new Micro-Electro-Mechanical-Systems (MEMS) device architectures with suspended metal membranes exploiting an innovative technological process based on the dry etching of silicon as sacrificial layer (e.g. polycrystalline and amorphous silicon).

Two non-limitative embodiments of the invention will be disclosed hereafter :

## 1) The Suspended-Gate MOSFET with Metal-Over-Gate Architecture with Full-Dry Etching Process

### Background of the invention (SG-MOSFET)

The suspended or movable gate Metal Oxide Semiconductor Field Effect Transistor (SG-MOSFET) has been extensively reported in the literature and a number of device architectures have been disclosed for various applications (see patents [P-SG1] – [P-SG13] and publications [SG1] – [SG8]). None of the types of inventions or publications referred hereto use architectures with metal-over-gate SG-MOSFET and a dry technological process to release it that are objects of this invention. The material of the suspended gate of previous reports is polycrystalline silicon (polysilicon) and the sacrificial layers are silicon oxide ($SiO_2$) or polymers and none proposed silicon as sacrificial layer. Also, most part of publications and patents use wet etching to release the suspended structures, which is in contrast with our technique proposed here. The main applications are gas or pressure sensors and accelerometers. Some accelerometer previously proposed exploited the lateral or vertical displacement of the gate but their architectures are different from our proposal. None of the referred patents and publications, except our publications [SG6] – [SG8] referred to the use of SG-

MOSFET for RF switches and capacitors, nor as a suspended-gate magnetic sensor SG-MAGFET.

## Patents related to similar devices:

| | | |
|---|---|---|
| [P-SG1]US 6,204,544 | Louisiana State Univ. | Mar. 2001 |
| [P-SG2]US 6,220,096 | Interscience, Inc. | Apr. 2001 |
| [P-SG3]US 5,874,675 | Interscience, Inc. | Feb 1999 |
| [P-SG4]US 6,043,524 | Motorola, Inc. | Mar. 2000 |
| [P-SG5]US 5,903,038 | Motorola, Inc. | May 1999 |
| [P-SG6]US 5,818,093 | Motorola, Inc. | Oct. 1998 |
| [P-SG7]US 5,600,065 | Motorola, Inc. | Feb. 1997 |
| [P-SG8]US 5,181,156 | Motorola, Inc. | Jan. 1993 |
| [P-SG9]US 5,786,235 | Siemens | Jul. 1998 |
| [P-SG10] US 5,627,397 | Nippondenso Co., Ltd. | May 1997 |
| [P-SG11] US 5,541,437 | Nippondenso Co., Ltd. | Jul. 1996 |
| [P-SG12] US 4,906,586 | Cornell Research Foundation, Inc. | Mar. 1990 |
| [P-SG13] US 4,812,888 | Cornell Research Foundation, Inc. | Mar. 1989 |

## Publications related to similar devices:


[SG1] E. Hynes, P. Elebert, D. McAuliffe, et al., "The CAP-FET, a scaleable MEMS sensor technology on CMOS with programmable floating gate", presented at International Electron Devices Meeting, 2001, pp. 917-920.

[SG2] D. M. Edmans, A. Gutierrez, C. Corneau, et al., "Micromachined accelerometer with a movable gate transistor sensing element", *Proceedings of SPIE*, 3224, 1997, pp. 314-324.

[SG3] J. T. Suminto and W. H. Ko, "Pressure-sensitive insulated gate field-effect transistor (PSIGFET)", *Sensors and Actuators*, A21-23, 1990, pp. 126-132.

[SG4] A. Yoshikawa, "Properties of a movable-gate-field-effect structure as an electromechanical sensor", *Journal of Acoustical Society of America*, 64, 1978, pp. 725-730.

[SG5] H. C. Nathanson, W. E. Newell, R. A. Wickstrom, et al., "The resonant gate transistor", *IEEE Transactions on Electron Devices*, 14(3), 1967, pp. 117-133.

[SG6] A.M. Ionescu, "MEMS for Reconfigurable Wide-Band RF ICs", Proceedings of SBMICRO 2001, Pirenopolis, Brasil, September 2001.

[SG7] V. Pott, A. M. Ionescu, R. Fritschi, et al., "The suspended-gate MOSFET (SG-MOSFET): a modeling outlook for the design of RF MEMS switches and tunable capacitors", presented at International Semiconductor Conference (CAS '01), Sinaia, Romania, Oct. 2001, pp. 137-140.

[SG8] A. M. Ionescu, V. Pott, R. Fritschi, K. Banerjee, M. J. Declercq, Ph. Renaud, C. Hibert, Ph. Fluckiger and G.-A. Racine, "Modeling and design of a low-voltage SOI Suspended-Gate MOSFET (SG-MOSFET) with a metal-over-gate-architecture", IEEE International Symposium on Quality Electronic Design (ISQED), San Jose, CA, March 18-21, 2002 (to appear).

## Brief description of the drawings

**FIG. 1**: Cross sections of the suspended-gate MOSFET: (a) architecture on Silicon-On-Insulator, (b) architecture on silicon substrate and (c) architecture with the underneath silicon substrate etched. The gate is made of metal in all cases and its displacement is vertical.

**FIG. 2**: Upper view (Scanning Electron Microscopy images) of SG-MOSFETs with three different designs of the suspension metal arms.

**FIG. 3**: Design of a SG-MOSFET with lateral Hall contacts for silicon magnetic sensor with tuneable sensitivity.

**FIGS. 4.1-4.11**: Detailed description of the SG-MOSFET technological process.

## Description of the SG-MOSFET architecture and principle

The cross section and the principle of the SG-MOSFET are depicted in Figs. 1: it combines in a top-down architecture a suspended metal membrane used as movable gate with a MOS transistor. This architecture is nor a pure MEMS device nor a pure solid-state device, but a hybrid combination of both. When its gate voltage, $V_g$, is increased, the intrinsic gate-voltage, $V_{gint}$, which drives the MOS channel formation, is tuned according to a capacitor divider:

$$V_{gint} = \frac{V_g}{1 + C_{gcint} / C_{gap}}$$

where $C_{gcint}$, $C_{gap}$ are the intrinsic gate-to-channel capacitance of the underneath MOSFET and the air-gap capacitance, respectively. The membrane moves continuously downwards as long as the equilibrium is maintained between electrostatic and elastic forces:

$$|F_{elastic}| = kx = \frac{1}{2} \frac{\varepsilon_{air} A (V_g - V_{gint})^2}{(t_{gap0} - x)^2} = |F_{electr}|$$

where k is the equivalent elastic constant of the gate, x is the gate displacement, , $t_{gap0}$ the initial air-gap dimension and $V_{gint}$ the intrinsic (or internal) gate voltage. When $V_g$ equals the pull-in voltage, $V_{PI}$, unstable equilibrium is reached and the switch (suspended membrane) moves from the 'off' to the 'on' state.

Some unique characteristics of the SG-MOSFET are mentioned below:

(i) the *dynamic threshold voltage*: low in the 'on' state and high in the 'off' state, which is a key advantage for RF switch use because of a higher isolation in the 'off' state compared to the solid-state MOSFET;

(ii) the *super-exponential* dependence of $Q_{inv}$ vs. $V_g$ in the sub-threshold region, that can result in local sub-threshold slope better than the ideal limit of 60mV/decade of any conventional MOSFET and the *super-linear* dependence of $Q_{inv}$ vs. $V_g$ in moderate and strong inversions;

(iii) the possibility to provide RF switches with capacitive rations between on and off state better than 100;

(iv) the possibility to use the SG-MOSFET as tuneable capacitor with tuning range better than any other similar MEMS capacitor.

In reference [SG8] we have proposed the first unified analytical model of this device, including all regimes of operation.

The key parameters of the SG-MOSFET architecture depicted in FIGS. 1 and 2 are: the thickness of the initial air-gap, the thickness of Insulator 1, the thickness of Insulator 2, the equivalent elastic constant k depending of the arm material and on their design, the surface of the metal suspended gate membrane.

FIGS. 2 a, b, c present some typical designs of the suspensions arms of the movable gate that directly impact on the equivalent k constant and then, on the value of the voltage needed to control the operation of the device: switching between on and off states or tuning of the gate capacitance. With the architecture and the technological process proposed herewith, the device operation can be achieved with voltages less that 5V, which makes it totally compatible with CMOS.

**Description of SG-MOSFET applications**

The following applications of the SG-MOSFET are proposed:

1. SG-MOSFET as Radiofrequency (RF) MEMS capacitive (contactless) switch when the gate is electrostatically moved from off (up) to on (down) states;
2. SG-MOSFET as Radiofrequency (RF) MEMS tuneable capacitor when the gate is electrostatically moved under equilibrium;
3. SG-MOSFET as MOSFET current switch when the gate is electrostatically switched between off and on states;
4. SG-MOSFET as integrated CMOS accelerometer wherein the acceleration is converted in vertical gate displacement and furthermore in variation of the drain current based on unique device;
5. SG-MOSFET as magnetic field sensor (MAGFET) with tuneable sensitivity to a magnetic field perpendicular to the gate surface, accordingly to the displacement of the suspended gate under electrostatic forces.

**Description of the SG-MOSFET technological process**

The fabrication of a SG-MOSFET in accordance with the present invention will be described with reference to FIGS. 4.1 to 4.11. The method of fabrication presented here is fully compatible with standard CMOS processes. A silicon substrate **01** is initially cleaned by conventional techniques and a field oxide layer **02**, those thickness is about 500nm, is grown in a wet atmosphere. Substrate **01** is <100> p-type silicon having a resistivity between 0.1-0.5 Ωcm. Alternatively, n-type Si substrate can also be used. Silicon-on-insulator (SOI) substrates are preferably used for RF applications to have high resistivity substrates. Using conventional photolithography techniques, the active device areas are formed by wet etching in a BHF (7:1) solution. The resulting structure is shown in FIG. 4.1.

The substrate **01** is then cleaned and a gate oxide layer **03** is thermally grown in a dry atmosphere as shown in FIG. 4.2. The thickness range is between 100 to 1000 A.

Next, as shown in FIG. 4.3, a silicon sacrificial layer **04** is deposited on the surface of the structure. The sacrificial layer **04** can be amorphous silicon or

polysilicon. Amorphous silicon is deposited by different kind of techniques: physical vapor deposition techniques, i.e. evaporation; RF or DC sputtering, and chemical vapor deposition techniques, i.e. low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). Polysilicon is deposited by LPCVD but can also be obtained from amorphous silicon after thermal annealing. The thickness range is between 100 nm to 2 μm. As shown in FIG. 4.4, the sacrificial layer **04** is then covered by a $SiO_2$ diffusion barrier layer **05**, those thickness is comprised between 1 nm to 100 nm. This layer prevents diffusion between the Si sacrificial layer **04** and the aluminum metal gate membrane **07**. The barrier layer **05** can be obtained by dry oxidation of the Si sacrificial layer **04** or by deposition of a $SiO_2$ layer even by RF sputtering or by LPCVD (low temperature oxide (LTO): $SiO_2$, phosphosilicate glass (PSG) or borophosphosilicate glass (BPSG)). Using conventional photolithography techniques, the diffusion barrier layer **05** is patterned even by wet etching in BHF or HF solution or by dry etching technique based on $C_xF_y$ RIE plasma process as shown in FIG. 4.5. The patterning of Si sacrificial layer **04** have to be anisotropic and highly selective on thin gate oxide **03**. This can be performed by cryogenic $SF_6/O_2$ chemistry process or chlorine-based chemistry using inductively coupled plasma (ICP) reactors. The resulting structure is shown in FIG. 4.6.

Then, as shown in FIG. 4.7, source and drain regions **06** are formed in silicon substrate **01** using conventional self-aligned process. It should be noted that our Si sacrificial layer **04** plays the role of polysilicon gate in standard CMOS processes. Phosphorus or arsenic ions are implanted in case of p-type substrate to formed n-doped source and drain regions **06**. For example, phosphorous ions are implanted at an energy of 25 keV and a dose of $2x10^{15}$ ions/cm$^2$. Alternatively, boron ions are implanted for n-type substrate to formed p-doped source and drain regions **06**. The structure is then annealed in a nitrogen atmosphere, to avoid the oxidation of the silicon sacrificial layer **04** side walls, at 950°C, to repair damage to silicon substrate **01** due to implantation.

Next, as shown in FIG. 4.8, the gate oxide layer **03** is patterned by wet etching in a BHF solution to open contact holes to source and drain regions **06**. Similarly, holes to contact the substrate **01** are opened.

The metal gate membrane layer **07** is then deposited on the surface of the structure as shown in FIG. 4.9. This layer also served as metal contacts to source and drain regions **06** and to substrate **01**. For example, a 0.8μm thick aluminum-silicon (with 1% silicon) is deposited by sputtering. Using conventional photolithography techniques, the aluminum gate membrane and the suspension arms are patterned by chlorine-based plasma chemistry or by wet etching in a standard ANP solution. The resulting structure is shown in FIG. 4.10.

The accelerometer application of SG-MOSFET needs a higher mass of the gate membrane in order to increase sensor sensitivity to acceleration without changing the rigidity of the suspension arms. This can be done by depositing a thicker metal layer **07**. Then, the metal gate membrane is patterned by partial etching of the metal layer **07**. After another photolithographic step, the suspension beams are formed.

Finally, the suspended metal gate membranes are released by dry etching in a fluorine-based chemistry with high selectivity to $SiO_2$ thin gate oxide layer **03** and metal layer **07**, as shown in FIG. 4.11.

## 2) The Metal-Metal MEMS RF Switch and Tuneable Capacitor Architecture with Full-Dry Etching Process

### Background of the invention (RF MEMS switch and tuneable capacitor)

The previously mentioned works have been dedicated to RF MEMS capacitive switches and RF tuneable capacitors, the architecture of which is very similar. Generally, the proposed architectures include a conductive region, a membrane and a dielectric between these two layers.

The tuneable MEMS capacitors exploits the equilibrium between electrosatic and elastic forces and the related conductive membrane displacement provides the tuning of the overall capacitor.

The switch has two states 'off' and 'on', the late one obtained by pulling down the movable membrane with an applied voltage. The MEMS switches have advantages in terms of low power consumption, low cost, linearity and compatibility with integrated circuits.

We proposed an architecture using two metal layers that can be used both for capacitive RF switch and tuneable MEMS capacitor. It includes two dielectric layers, each in contact with one of the metals. The upper dielectric is not mandatory and same structure can be used for same applications without this layer: it can however offer some advantages, at least in terms of extended stability of the structure. Our structure is released with dry etching of sacrificial silicon, which has never been proposed in the referred publications, and is fully compatible with CMOS and has a low voltage actuation.

### Patents related to tuneable capacitors

| | | |
|---|---|---|
| [P-TC1] WO 0,156,046 | Intel, Corp. | Aug. 2001 |
| [P-TC2] WO 0,161,848 | Nokia Mobile Phones, Ltd | Aug. 2001 |
| [P-TC3] WO 0,145,127 | MCNC | Jul. 2001 |
| [P-TC4] US 5,959,516 | Rockwell Science Center LLC | Sept. 1999 |
| [P-TC5] US 5,880,921 | Rockwell Science Center LLC | Mar. 1999 |

## Publications related to RF tuneable capacitors


[TC1] Young, D. J. and B. E. Boser, "A micromachined variable capacitor for monolithic low-noise VCO's", presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, 1996, pp. 86-89.

[TC2] Young, D. J. and B. E. Boser, "A micromachine-based RF low-noise voltage-controlled oscillator", presented at IEEE Custom Integrated Circuits Conference, 1997, pp. 431-434.

[TC3] Zou, J., C. Liu, J. Schutt-Aine, et al., "Development of a wide tuning range MEMS tunable capacitor for wireless communication systems", presented at International Electron Devices Meeting, 2000, pp. 403-406.

[TC4] Zou, J. and C. Liu, "Development of a novel micro electromechanical tunable capacitor with a high tuning range", presented at 58th Device Research Conference, 2000, pp. 111-112.

[TC5] Dec, A. and K. Suyama, "Micromachined electro-mechanically tunable capacitors and their applications to RF IC's", *IEEE Transactions on Microwave Theory and Techniques*, 46 (12), 1998, pp. 2587-2596.

[TC6] Larson, L. E., R. H. Hackett, M. A. Melendes, et al., "Micromachined microwave actuator (MIMAC) technology: a new tuning approach for microwave integrated circuits", presented at IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1991, pp. 27-30.

[TC7] Yao, J. J., S. Park and J. DeNatale, "High tuning-ratio MEMS-based tunable capacitors for RF communications applications", presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, 1998, pp. 124-127.

[TC8] Hung, E. S. and S. D. Senturia, "Tunable capacitors with programmable capacitance-voltage characteristic", presented at Solid-State Sensor and Actuator Workshop, Hilton Head Island, SC, 1998, pp. 292-295.

[TC9] Park, J. Y., H.-T. Kim, Y. Kwon, et al., "A tunable millimeter-wave filter using coplanar waveguide and micromachined variable capacitors", presented at 10th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '99), Sendai, Japan, 1999, pp. 1272-1275.

[TC10] Yoon, J.-B. and C. T.-C. Nguyen, "A high-Q tunable micromechanical capacitor with movable dielectric for RF applications", presented at International Electron Devices Meeting, 2000, pp. 489-492.

[TC11] Fan, L., R. T. Chen, A. Nespola, et al., "Universal MEMS platforms for passive RF components: suspended inductors and variable capacitors", presented at 11th Annual International Workshop on Micro Electro Mechanical Systems (MEMS '98), 1998, pp. 29-33.

[TC12] Wu, H. D., K. F. Harsh, R. S. Irwin, et al., "MEMS designed for tunable capacitors", presented at IEEE MTT-S International Microwave Symposium, 1998, pp. 127-129.

[TC13] Harsh, K. F., B. Su, W. Zhang, et al., "The realization and design considerations of a flip-chip integrated MEMS tunable capacitor", *Sensors and Actuators A*, 80 (2), 2000, pp. 108-118.

[TC14] Feng, Z., W. Zhang, B. Su, et al., "Design and modeling of RF MEMS tunable capacitors using electro-thermal actuators", presented at IEEE MTT-S International Microwave Symposium, 1999, pp. 1507-1510.

## Patents related to RF switches

| | | |
|---|---|---|
| [P-SW1] US 5,619,061 | Texas Instruments, Inc. | Apr. 1997 |
| [P-SW2] WO 0,031,819 | Raytheon, Co | Jun. 2000 |
| [P-SW3] US 6,307,519 | Hughes Electr., Corp.; Raytheon, Co | Oct. 2001 |
| [P-SW4] US 6,143,997 | Univ. Illinois, Urbana-Champaign | Nov. 2000 |

## Publications related to RF switches

[SW1] S. Barker and G. M. Rebeiz, "Distributed MEMS true-time delay phase shifters and wide-band switches", *IEEE Transactions on Microwave Theory and Techniques*, 46(11, Part 2), 1998, pp. 1881-1890.

[SW2] C.-L. Dai, K. Yen and P.-Z. Chang, "Applied electrostatic parallelogram actuators for microwave switches using the standard CMOS process", *Journal of Micromechanics and Microengineering*, 11(6), 2001, pp. 697-702.

[SW3] C. Goldsmith, T.-H. Lin, B. Powers, et al., "Micromechanical membrane switches for microwave applications", presented at IEEE MTT-S International Microwave Symposium, 1995, pp. 91-94.

[SW4] C. Goldsmith, J. Randall, S. Eshelman, et al., "Characteristics of micromachined switches at microwave frequencies", presented at IEEE MTT-S International Microwave Symposium, 1996, pp. 1141-1144.

[SW5] C. L. Goldsmith, Z. Yao, S. Eshelman, et al., "Performance of low-loss RF MEMS capacitive switches", *IEEE Microwave and Guided Wave Letters*, 8(8), 1998, pp. 269-271.

[SW6] K. Grenier, B. P. Barber, V. Lubecke, et al., "Integrated RF MEMS for single chip radio", presented at 11th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '01) and EUROSENSORS XV, Munich, Germany, 2001, pp. 1528-1531.

[SW7] D. Hyman and M. Mehregany, "Contact physics of gold microcontacts for MEMS switches", presented at 44th IEEE Holm Conference on Electrical Contacts, 1998, pp. 133-140.

[SW8] D. Hyman, A. Schmitz, B. Warneke, et al., "GaAs-compatible surface-micromachined RF MEMS switches", *Electronics Letters*, 35(3), 1999, pp. 224-226.

[SW9] D. Hyman and M. Mehregany, "Contact physics of gold microcontacts for MEMS switches", *IEEE Transactions on Components and Packaging Technologies*, 22(3), 1999, pp. 357-364.

[SW10] J. Kim, W. Shen, L. Latorre, et al., "A micromechanical switch with electrostatically driven liquid-metal droplet", presented at 11th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '01) and EUROSENSORS X, Munich, Germany, 2001, pp. 748-751.

[SW11] J. B. Muldavin and G. M. Rebeiz, "30 GHz tuned MEMS switches", presented at IEEE MTT-S International Microwave Symposium, 1999, pp. 1511-1514.

[SW12] J. B. Muldavin and G. M. Rebeiz, "High-isolation CPW MEMS shunt switches. 2. Design", *IEEE Transactions on Microwave Theory and Techniques*, 48(6), 2000, pp. 1053-1056.

[SW13] J. B. Muldavin and G. M. Rebeiz, "High-isolation CPW MEMS shunt switches. 1. Modeling", *IEEE Transactions on Microwave Theory and Techniques*, 48(6), 2000, pp. 1045 -1052.

[SW14] J. B. Muldavin and G. M. Rebeiz, "High-isolation inductively-tuned X-band MEMS shunt switches", *IEEE MTT-S International Microwave Symposium*, 1, 2000, pp. 169-172.

[SW15] B. R. Norvell, R. J. Hancock, J. K. Smith, et al., "Micro electro mechanical switch (MEMS) technology applied to electronically scanned arrays for space based radar", presented at IEEE Aerospace Conference, 1999, pp. 239-247.

[SW16] S. P. Pacheco, L. P. B. Katehi and C. T.-C. Nguyen, "Design of low actuation voltage RF MEMS switch", presented at IEEE MTT-S International Microwave Symposium, 2000, pp. 165-168.

[SW17] J. Y. Park, G. H. Kim, K. W. Chung, et al., "Fully integrated micromachined capacitive switches for RF applications", presented at IEEE MTT-S International Microwave Symposium, 2000, pp. 283-286.

[SW18] J. Y. Park, G. H. Kim, K. W. Chung, et al., "Electroplated RF MEMS capacitive switches", presented at 13th Annual International Conference on Micro Electro Mechanical Systems (MEMS '00), 2000, pp. 639-644.

[SW19] J. Y. Park, K. Kang, N. Kang, et al., "A 3-voltage actuated micromachined RF switch for telecommunications applications", presented at 11th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '01) and EUROSENSORS XV, Munich, Germany, 2001, pp. 1540-1543.

[SW20] K. E. Petersen, "Micromechanical membrane switches on silicon", *IBM Journal of Research and Development*, 23(4), 1979, pp. 376-385.

[SW21] F. Plötz, S. Michaelis, G. Fattinger, et al., "Performance and dynamics of a RF MEMS switch", presented at 11th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '01) and EUROSENSORS XV, Munich, Germany, 2001, pp. 1560-1563.

[SW22] J. Rizk, G.-L. Tan, J. B. Muldavin, et al., "High-isolation W-band MEMS switches", *IEEE Microwave and Wireless Components Letters*, 11(1), 2001, pp. 10-12.

[SW23] I. Schiele and B. Hillerich, "Comparison of lateral and vertical switches for application as microrelays", *Journal of Micromechanics and Microengineering*, 9(2), 1999, pp. 146-150.

[SW24] S.-C. Shen and M. Feng, "Low actuation voltage RF MEMS switches with signal frequencies from 0.25 GHz to 40 GHz", presented at International Electron Devices Meeting, 1999, pp. 689-692.

[SW25] J. K. Smith, F. W. Hopwood and K. A. Leahy, "MEM switch technology in radar", presented at IEEE International Radar Conference, 2000, pp. 193-198.

[SW26] K. Suzuki and A. Pauly, "Theoretical analysis of the tilting effect in silicon micro-switches", presented at 11th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '01) and EUROSENSORS XV, Munich, Germany, 2001, pp. 244-247.

[SW27] H. A. C. Tilmans, H. Ziad, H. Jansen, et al., "Wafer-level packaged RF-MEMS switches fabricated in a CMOS fab", presented at International Electron Devices Meeting, 2001, pp. 921-924.

[SW28] M. Ulm, T. Walter, R. Mueller-Fiedler, et al., "K-band capacitive MEMS-switches", *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, 2000, pp. 119-122.

[SW29] M. Ulm, M. Reimann, T. Walter, et al., "Scalability of capacitive RF MEMS switches", presented at 11th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '01) and EUROSENSORS XV, Munich, Germany, 2001, pp. 1536-1539.

[SW30] J. J. Yao and M. F. Chang, "A surface micromachined miniature switch for telecommunications applications with signal frequencies from DC up to 4.GHz", presented at 8th International Conference on Solid-State Sensors and Actuators (TRANSDUCERS '95), Stockholm, Sweden, 1995, pp. 384-387.

[SW31] Z. J. Yao, S. Chen, S. Eshelman, et al., "Micromachined low-loss microwave switches", *Journal of Microelectromechanical Systems*, 8(2), 1999, pp. 129-134.

[SW32] P. M. Zavracky, S. Majumder and N. E. McGruer, "Micromechanical switches fabricated using nickel surface micromachining", *Journal of Microelectromechanical Systems*, 6(1), 1997, pp. 3-9.

## Brief description of the drawings

FIG. 5 (a) Cross section and principle of the metal-metal tuneable MEMS capacitor or switch provided by the full dry etching of sacrificial amorphous silicon and (b) upper view of a metal-metal tuneable MEMS capacitor.

FIGS. 6.1-6.10: Detailed description of the tuneable metal-metal MEMS capacitor technological process.

## Description of the metal-metal MEMS switch and tuneable capacitor architecture and principle

The cross section of the proposed device is in FIG. 5: it uses two metal layers, capped with two insulators separated by two different air-gaps (Airgap 1 and Airgap 2). Metal 1 is deposited on top of another insulator called Insulator 0 that can be SiO2 or Si3N4. The movable metal membrane is defined by Metal 2 and its vertical displacement is controlled by the voltage applied between lateral electrodes E1 et E2. The active area of the capacitor or switch is defined by the central electrode EC that drives the RF signal.

One advantage relates to the difference between Airgap 1 and Airgap 2 (Airgap 1 is designed larger than Airgap 2), thus, the capacitor tuning range is significantly enlarged because the equilibrium region between electrostatic and elastic forces is enlarged.

The difference with respect to other publications that proposes also the use of two air-gaps is that, our architecture uses two insulator layers over the metals, resulting in different characteristics, and the releasing process is completely different, with amorphous silicon as sacrificial layer. Moreover much more aggressively scaled dimensions in terms of air-gaps can be addressed with our structure. Advantages of better yield and fully compatible CMOS process can be mentioned. Also, by the proper design of the suspension arms (with meanders), a low voltage, CMOS-compatible, operation can be achieved for this structure. Membranes have etch holes to give access to the Si sacrificial layer and so increase the releasing rate (see FIG. 5 b).

This structure can be used for both MEMS RF switch and tuneable capacitor applications. The lateral electrodes E1 and E2 can be also eliminated and the DC and RF signals superposed.

**Description of metal-metal MEMS device applications**

The following applications of the metal-metal MEMS device architecture are proposed:

1. Radiofrequency (RF) MEMS capacitive (contactless) switch when the gate is electrostatically moved from off (up) to on (down) states;
2. Radiofrequency (RF) MEMS tuneable capacitor when the gate is electrostatically moved under equilibrium;
3. Integrated CMOS accelerometer wherein the acceleration is converted in vertical displacement of the membrane and furthermore in variation of the capacitance.

**Description of the metal-metal tuneable MEMS capacitor technological process**

The fabrication of metal-metal tunable capacitors and switches in accordance with the present invention will be described with reference to FIGS. 6.1 to 6.10. The method of fabrication presented here is fully compatible with CMOS post-processing. A silicon substrate **01** is initially cleaned by conventional techniques and a silicon dioxide layer **02** is grown in a wet atmosphere as shown in FIG. 6.1. The thickness range is between 0.2 to 2 μm. A low temperature oxide (LTO) deposited by LPCVD can replace the wet oxidation. Silicon-on-insulator (SOI) substrates are preferably used for RF applications to have high resistivity substrates.

Then, the first metal layer **03** is deposited on the surface as shown in FIG. 6.2. A 1 -μm thick aluminum-silicon layer (with 1% silicon) is sputtered. Using conventional photolithography techniques, the aluminum base electrodes and the contact pads are patterned by chlorine-based plasma chemistry or by wet etching in a standard ANP solution as shown in FIG. 6.3.

As shown in FIG. 6.4, the structures are then covered by a $SiO_2$ diffusion barrier layer **04**, the thickness of which is comprised between 10 to 100 nm. This layer will prevent diffusion between the silicon sacrificial layer **05** and the aluminum base electrodes. The barrier layer **04** can be obtained by deposition of a $SiO_2$ layer even by RF sputtering or by LPCVD (low temperature oxide (LTO): $SiO_2$, phosphosilicate glass (PSG).

Next, as shown in FIG. 6.5, an amorphous silicon sacrificial layer **05** is deposited on the surface of the structure. Amorphous silicon is deposited by different kind of techniques: physical vapor deposition techniques, i.e. evaporation, RF or DC sputtering, and plasma enhanced chemical vapor deposition (PECVD). The thickness range is between 100 nm to 3 μm.

The patterning of amorphous silicon sacrificial layer **05** is performed by isotropic fluorine-based chemistry process using inductively coupled plasma (ICP) reactors. Two photolithographic steps are needed to provide the three-dimensional membrane shape. The first step consists in thinning the silicon sacrificial layer **05** to define the RF capacitor as shown in FIG. 6.6. The second step consists in passing through the silicon sacrificial layer **05** to prepare the mechanical anchors to the substrate **01** for the suspended membranes. The resulting structure is shown in FIG. 6.7.

As shown in FIG. 6.8, the patterned sacrificial layer **05** is then covered by a $SiO_2$ diffusion barrier layer **06**, those thickness is comprised between 10 to 100nm. The second metal layer **07** is then deposited on the surface of the structure. A 1μm thick aluminum-silicon (with 1% silicon) is sputtered. Using conventional photolithography techniques, the aluminum membrane and the suspension beams are patterned even by chlorine-based plasma chemistry or by wet etching in a standard ANP solution. The resulting structure is shown in FIG. 6.9. Next, the diffusion barrier layer **06** is patterned by dry etching technique based on $C_xF_y$ RIE plasma process to have an access to silicon sacrificial layer **05**.

Then, the suspended metal membranes are released by dry etching of the silicon sacrificial layer **05** in a fluorine-based chemistry with a high selectivity to $SiO_2$ and aluminum as shown in FIG. 6.10. Finally, the diffusion barrier layer **04** on electric contacts is removed by anisotropic $C_xF_y$ RIE plasma process.

## Claims

1. A Metal-Oxide-Semiconductor Field Effect Transistor architecture with suspended metal gate and using one insulator over the channel (layer **3** in the technological process) and one insulator under and included with the metal suspended gate (layer **5** in the technological process);
2. The device of claim **1** to be fabricated on silicon, silicon-on-insulator and on silicon with the underneath substrate etched;
3. The device of claim **1** to be used as Radiofrequency (RF) MEMS capacitive (contactless) switch when the gate is electrostatically moved;
4. The device of claim **1** to be used as Radiofrequency (RF) MEMS tuneable capacitor when the gate is electrostatically moved;
5. The device of claim **1** to be used as current switch when the gate is electrostatically moved;
6. The device of claim **1** to be used as accelerometer wherein the acceleration is converted in vertical gate displacement and furthermore in variation of the drain current;
7. The device of claim **1** to be used as magnetic field sensor (MAGFET) with tuneable sensitivity accordingly to the displacement of the suspended gate under electrostatic forces;
8. The device of claim **1** used as a MOSFET with a sub-threshold slope better than 60 mV/decade, which is the theoretical limit of any solid-state MOSFET;
9. The device of claim **1** to be also used for the applications mentioned at claims **3, 4, 5, 6** and **7** without the insulator layer **5**;
10. A method of fabrication of the device of claim **1**, called SG-MOSFET, based on conventional MOSFET process steps with:
    - A suspended metal gate;
    - A Si sacrificial layer;
    - A dry fluorine-based chemistry releasing of the movable metal gate highly selective on $SiO_2$ thin gate oxide;
    - A possibility to fabricate the SG-MOSFET device on Si or SOI wafers;
11. Different kinds of said Si sacrificial layer of claim **10**: amorphous Si using LPCVD, sputtering, evaporation, PECVD techniques, polysilicon using

LPCVD technique, polysilicon from amorphous Si after a thermal process; silicon-germanium (SiGe);

12. The said metals of claim **10** are aluminium, AlSi, AlSiCu, copper, gold, tungsten, platinum, titanium and combinations of these metals;
13. The thickness of said Si sacrificial layer of claim **10** is 10 nm up to 10 µm;
14. An anti-diffusion $SiO_2$ barrier between the Si sacrificial layer and the movable metal membrane, the barrier can be obtained by different ways:
    - Dry oxidation of the Si sacrificial layer;
    - Deposition by sputtering or LTO furnace ($SiO_2$, PSG or BPSG);
15. Alternative techniques to etch the diffusion barrier:
    - Wet technique using BHF or HF acid;
    - Dry technique based on $C_xF_y$ RIE plasma process;
16. Different dry anisotropic patterning of the Si sacrificial layer highly selective on $SiO_2$ thin gate oxide based on:
    - Cryogenic $SF_6/O_2$ chemistry process using ICP plasma reactors;
    - Chlorine-based chemistry process using ICP plasma reactors;
17. Alternative techniques to dry etch the Si sacrificial layer for aluminum membrane releasing:
    - $SF_6$ remote plasma (ICP or ECR);
    - $XeF_2$ technique (without plasma);
18. The fabrication of P- or N-channel SG-MOSFET devices fully compatible with conventional CMOS process;
19. An increased tuning range of the tuneable capacitor application of device mentioned at claim **1**, limited only by the air-gap dimension, by using a constant capacitor connected in series with the SG-MOSFET gate;
20. The series capacitor mentioned at claim **18** is included in the movable gate and the use of the diffusion barrier for this purpose.
21. A MEMS device architecture using two metal levels, one fixed and one movable, called membrane, both capped with one insulator, with variable air-gaps and an underlying insulator deposited on a semiconductor substrate;
22. The device of claim **21** to be fabricated on silicon, silicon-on-insulator and on silicon with the underneath substrate etched;

23. The device of claim **21** to be used as Radiofrequency (RF) MEMS capacitive (contactless) switch when the said membrane is electrostatically moved between extreme positions;
24. The device of claim **21** to be used as Radiofrequency (RF) MEMS tuneable capacitor when the gate is electrostatically moved under equilibrium;
25. The device of claim **21** to be used as accelerometer wherein the acceleration is converted in vertical membrane displacement and furthermore in variation of the capacitance;
26. The device of claim **21** to be also used for the applications mentioned at claims **23, 24,** and **25** without one of insulator capping layers mentioned at claim **21**;
27. A method of fabrication of the device of claim **21** with:
    - A suspended metal membrane;
    - A fixed metal;
    - A Si sacrificial layer;
    - A dry fluorine-based chemistry releasing of the suspended metal membrane highly selective on $SiO_2$;
    - A possibility to fabricate the device on Si or SOI wafers;

28. The said Si sacrificial layer of claim **27**: amorphous Si using LPCVD, sputtering, evaporation, PECVD techniques;
29. The said metals of claim **27** are aluminium, AlSi, AlSiCu, copper, gold, tungsten, platinum, titanium and combinations of these metals;
30. The thickness of said Si sacrificial layer of claim **27** is 10nm up to 10μm.
31. An anti-diffusion $SiO_2$ barrier between the Si sacrificial layer and the movable metal membrane, the barrier can be obtained by different ways:
    - Dry oxidation of the Si sacrificial layer;
    - Deposition by sputtering or LTO furnace (SiO2, PSG or BPSG);

32. Alternative techniques to etch the diffusion barrier:
    - Wet technique using BHF or HF acid;

- Dry technique based on CxFy RIE plasma process;

33. Alternative techniques to dry etch the Si sacrificial layer for aluminum membrane releasing:
    - $SF_6$ remote plasma (ICP or ECR);
    - $XeF_2$ technique (without plasma);
34. The method of the said device at claim **21** is fully compatible with CMOS post-process;
35. An increased tuning range of the tuneable capacitor application of device mentioned at claim **21**, limited only by the air-gap dimension;
36. A series capacitor mentioned that can be included in the suspended membrane and can use the diffusion barrier for this purpose in order to increase the tuning range of the capacitor.

## Abstract

This invention concerns new Micro-Electro-Mechanical-Systems (MEMS) device architectures with suspended metal membranes exploiting an innovative technological process based on the dry etching of silicon as sacrificial layer (e.g. polycrystalline and amorphous silicon).

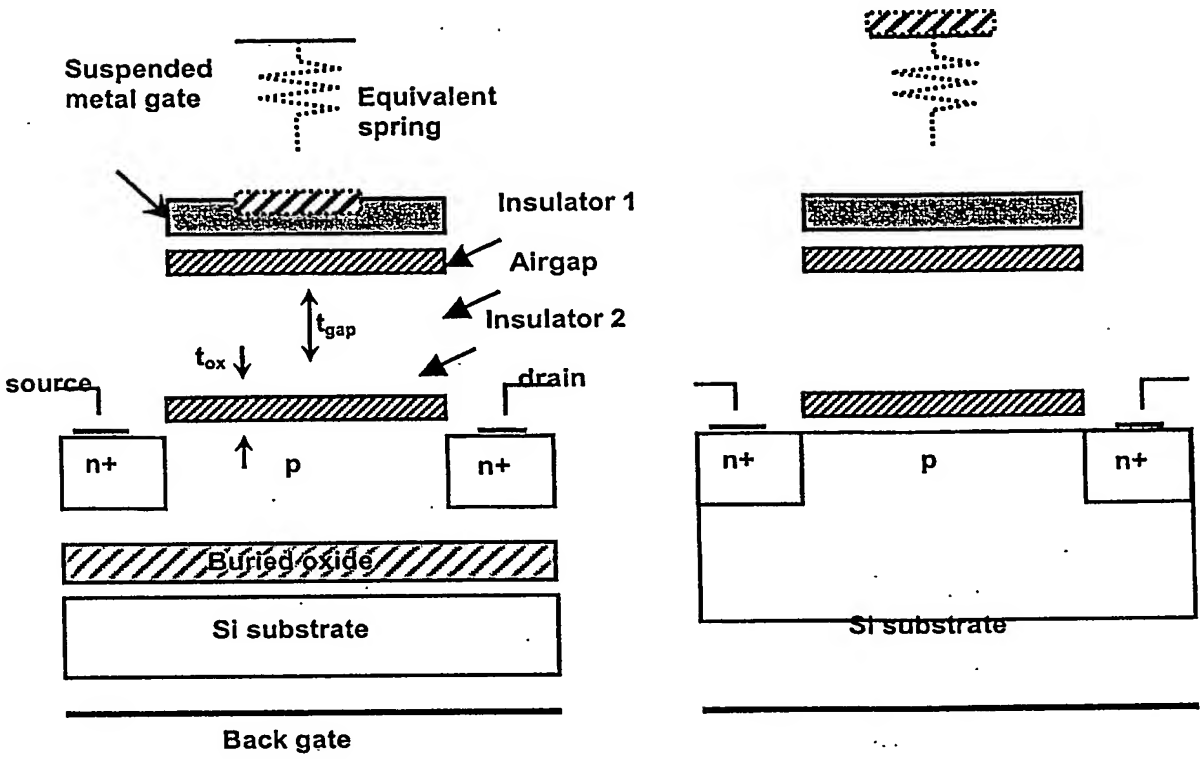
Two device architectures are in particular proposed and addressed with a full-dry etching process:

(1) a suspended-gate MOSFET with metal-over-gate architecture;

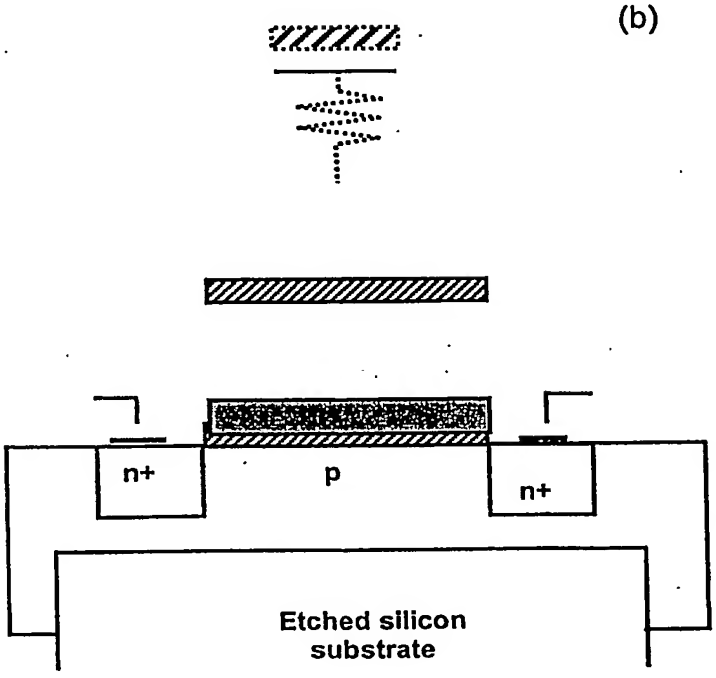
(2) a metal-metal MEMS RF switch and tuneable capacitor architecture.

The suspended-gate MOSFET architecture is proposed to be used as: (1) RF MEMS capacitive switch, by moving the suspended gate between two extreme positions, (2) RF MEMS tuneable capacitor, by moving the gate under equilibrium, (3) current switch, by switching on and off the subsequent MOSFET, (4) integrated accelerometer, by the vertical displacement of the gate under acceleration converted by the device in drain current variation, (5) magnetic field sensor with variable sensitivity, by moving vertically the suspended gate.

The metal-metal MEMS RF switch and tuneable capacitor architecture is proposed with a full-dry process using amorphous silicon as sacrificial layer.

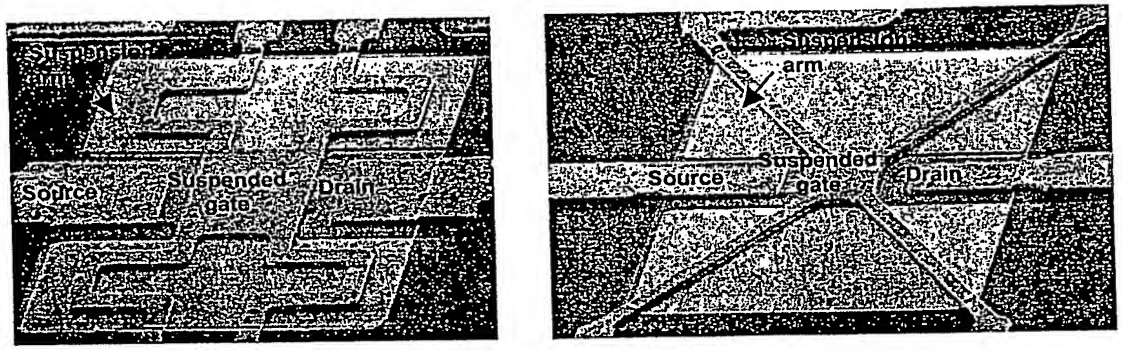

Suspended metal gate
Equivalent spring
Insulator 1
Airgap
Insulator 2
$t_{gap}$
$t_{ox}$
source
drain
n+
p
n+
Buried oxide
Si substrate
Back gate
n+
p
n+
Si substrate

(a) (b)

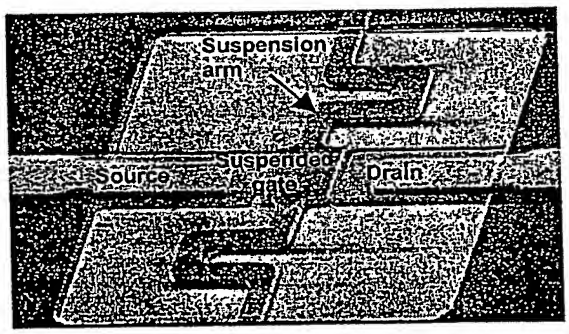

n+
p
n+
Etched silicon substrate

(c)

Fig. 1




(a) (b)




(c)

Fig. 2

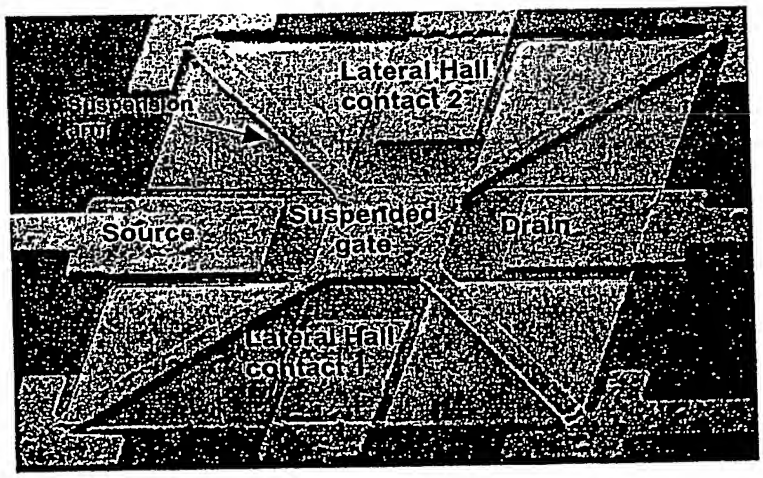



Fig. 3

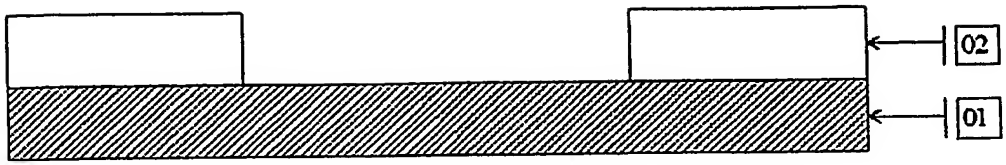



Fig. 4.1

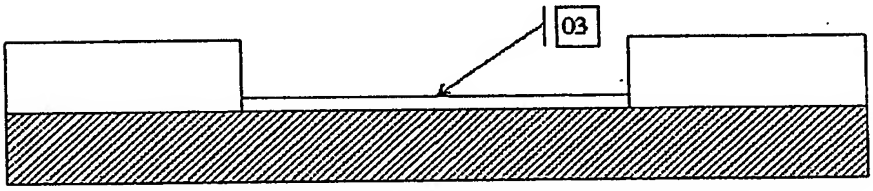



Fig. 4.2

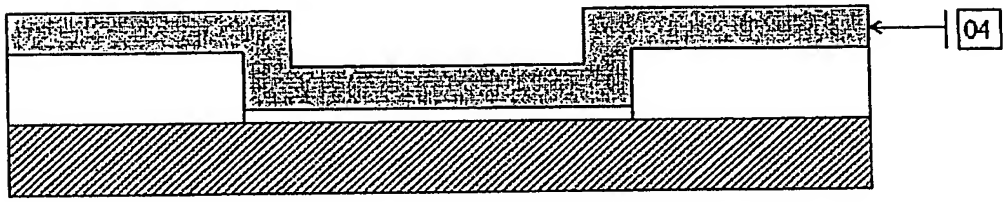



Fig. 4.3

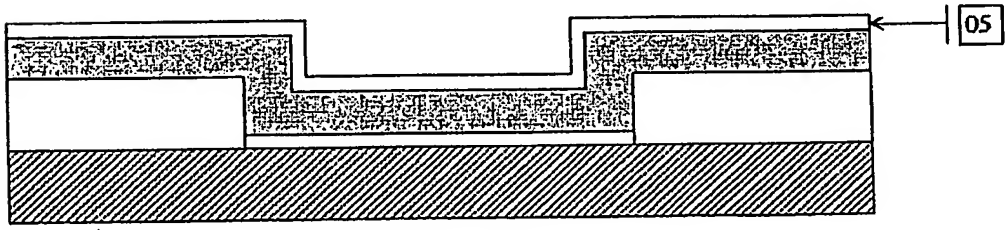



Fig. 4.4

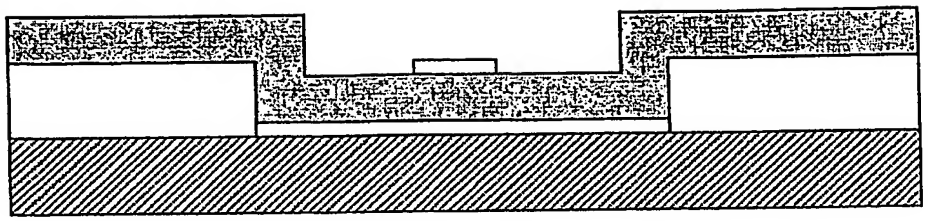


Fig. 4.5

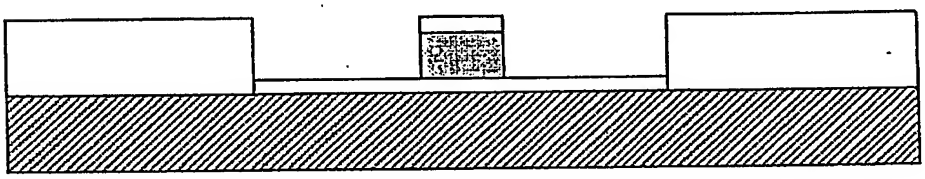


Fig. 4.6

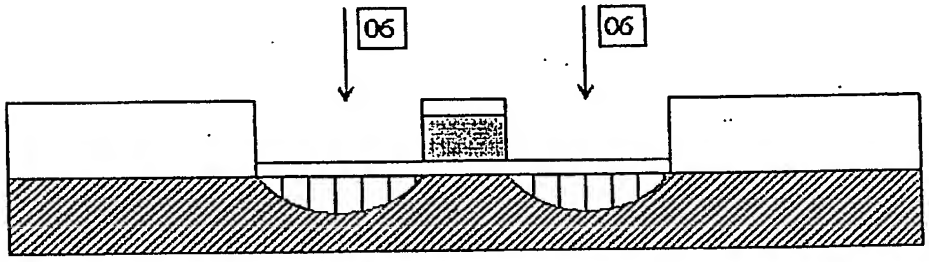



Fig. 4.7

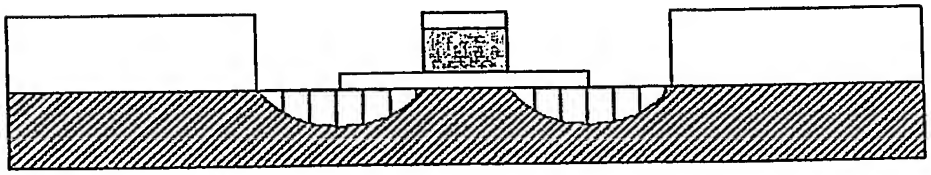


Fig. 4.8

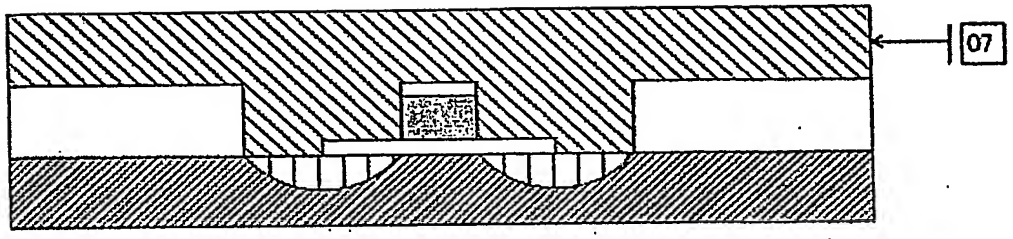



Fig. 4.9

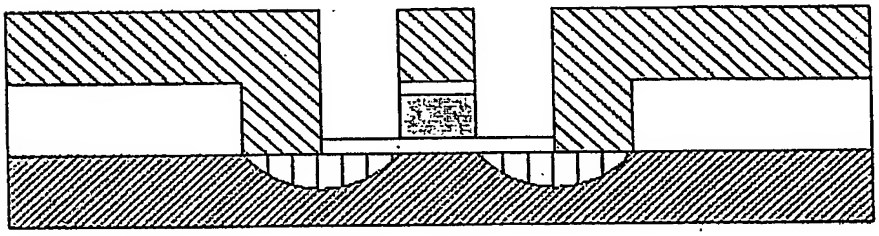


Fig. 4.10

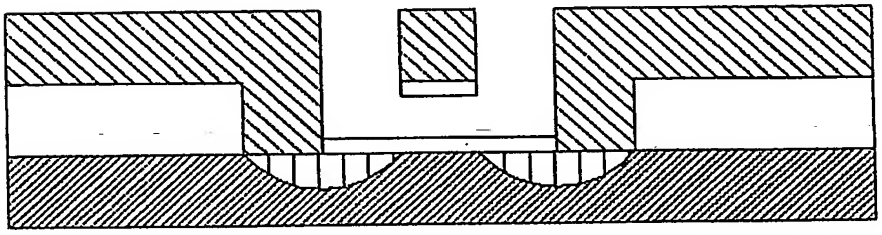
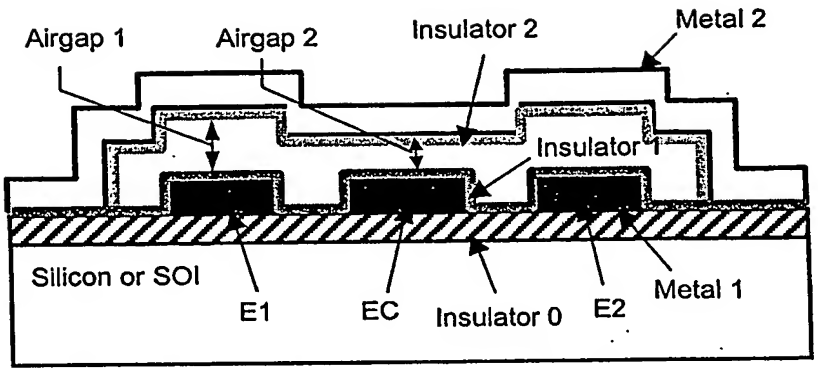
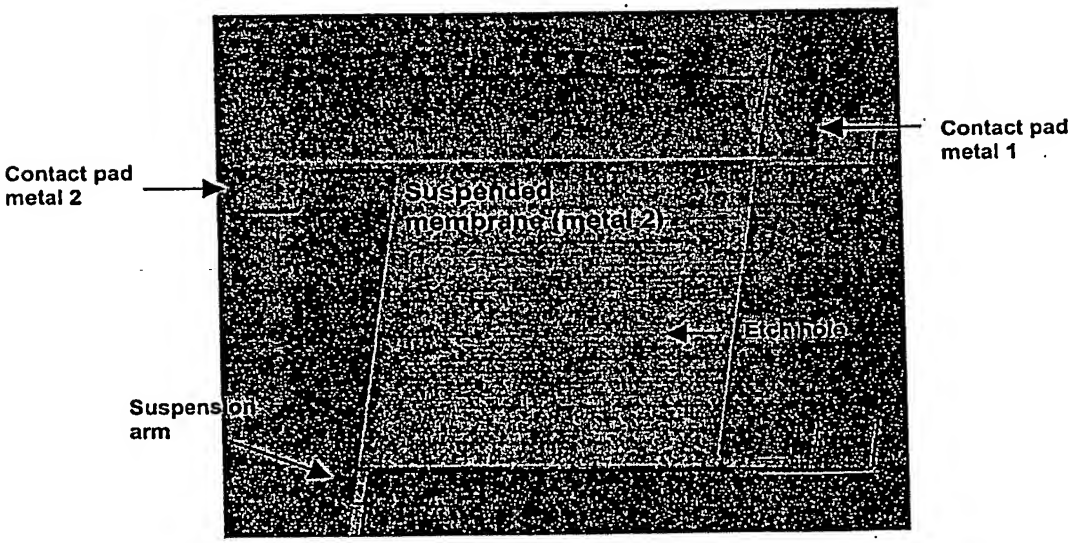


Fig. 4.11


Airgap 1
Airgap 2
Insulator 2
Metal 2
Insulator 1
Silicon or SOI
E1
EC
Insulator 0
E2
Metal 1

(a)


Contact pad metal 2
Suspended membrane (metal 2)
Contact pad metal 1
Etch hole
Suspension arm

(b)

**Fig. 5**

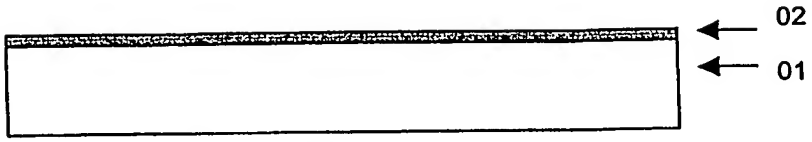



FIG. 6.1

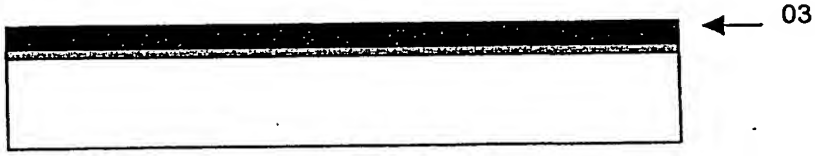



FIG. 6.2

FIG. 6.3

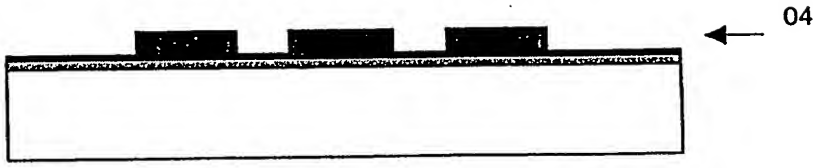
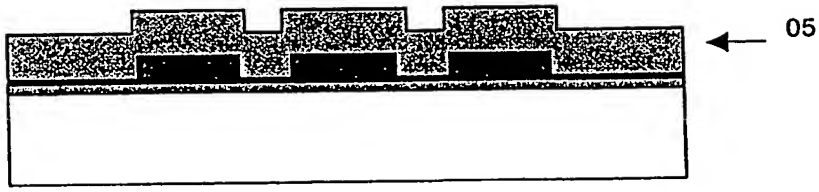



FIG. 6.4



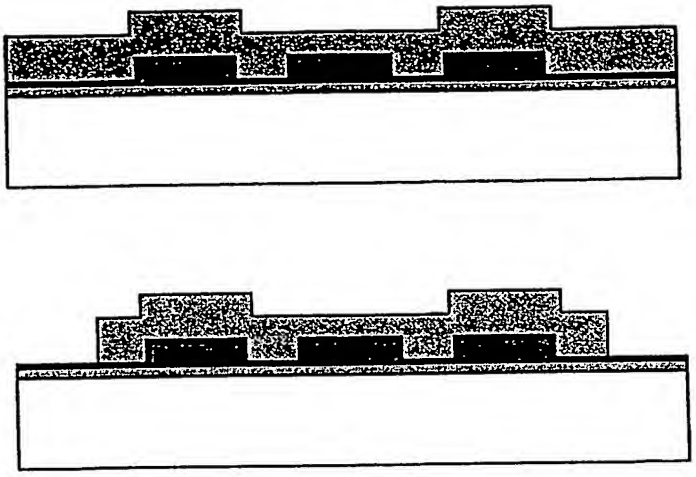


FIG. 6.6

FIG. 6.7

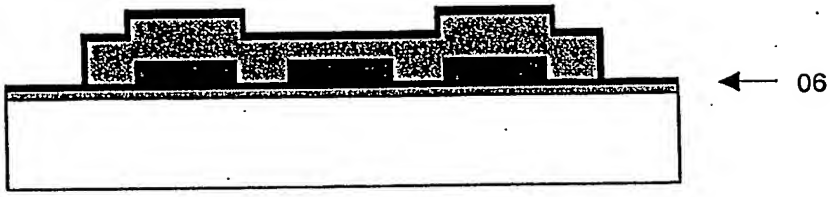



FIG. 6.8

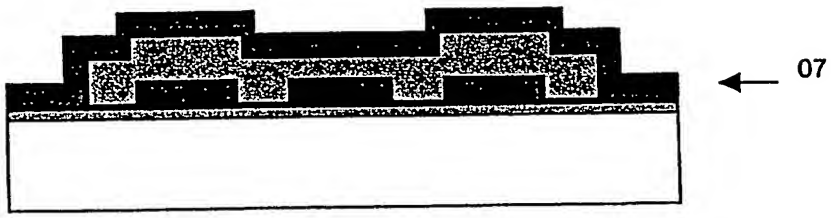



FIG. 6.9

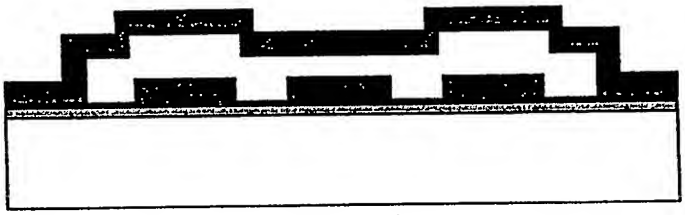


FIG. 6.10